## P3C1024

HIGH SPEED 128K x 8
3.3V STATIC CMOS RAM

## FEATURES

- 3.3 Volts Power Supply

■ High Speed (Equal Access and Cycle Times) - 15/17/20/25/35 ns (Commercial) - 20/25/35/45 ns (Industrial)

■ Single 3.3 Volts $\pm 0.3$ Volts Power Supply

- Easy Memory Expansion Using $\overline{\mathrm{CE}}_{1}, \mathrm{CE}_{2}$ and $\overline{O E}$ Inputs
■ Common Data I/O

■ Three-State Outputs
■ Fully TTL Compatible Inputs and Outputs
■ Advanced CMOS Technology

- Fast $t_{\mathrm{og}}$
- Automatic Power Down

■ Packages
-32-Pin DIP and SOJ

## DESCRIPTION

The P3C1024 is a 1,048,576-bit high-speed CMOS static RAM organized as 128 Kx 8 . The CMOS memory requires no clocks or refreshing, and has equal access and cycle times. Inputs are fully TTL-compatible. The RAM operates from a single $3.3 \mathrm{~V} \pm 0.3 \mathrm{~V}$ tolerance power supply.

Access times of 20 nanoseconds permit greatly enhanced system operating speeds. CMOS is utilized to reduce power consumption to a low level. The P3C1024 is a member of a family of PACE RAM ${ }^{\text {TM }}$ products offering fast access times.

The P3C1024 device provides asynchronous operations with matching access and cycle times. Memory locations are specified on address pins $\mathrm{A}_{0}$ to $\mathrm{A}_{16}$. Reading is accomplished by device selection ( $\overline{\mathrm{CE}}_{1}$ low and $C E_{2}$ high) and output enabling ( $\overline{\mathrm{OE})}$ while write enable $(\overline{\mathrm{WE}})$ remains HIGH. By presenting the address under these conditions, the data in the addressed memory location is presented on the data input/output pins. The input/output pins stay in the HIGH Z state when either $\overline{C E}_{1}$ or $\overline{\mathrm{OE}}$ is HIGH or $\overline{\mathrm{WE}}$ or $\mathrm{CE}_{2}$ is LOW.

Package options for the P3C1024 include 32-pin 300 mil DIP and SOJ packages as well as 400 mil SOJ.

FUNCTIONAL BLOCK DIAGRAM


PIN CONFIGURATION


